This material is based upon works supported by the Science Foundation Ireland under **Grant No. grant 15/IA/2880**

‘Off-the-Shelf’ FPGA/RF SoC Boards and Open-Source Tool-flows

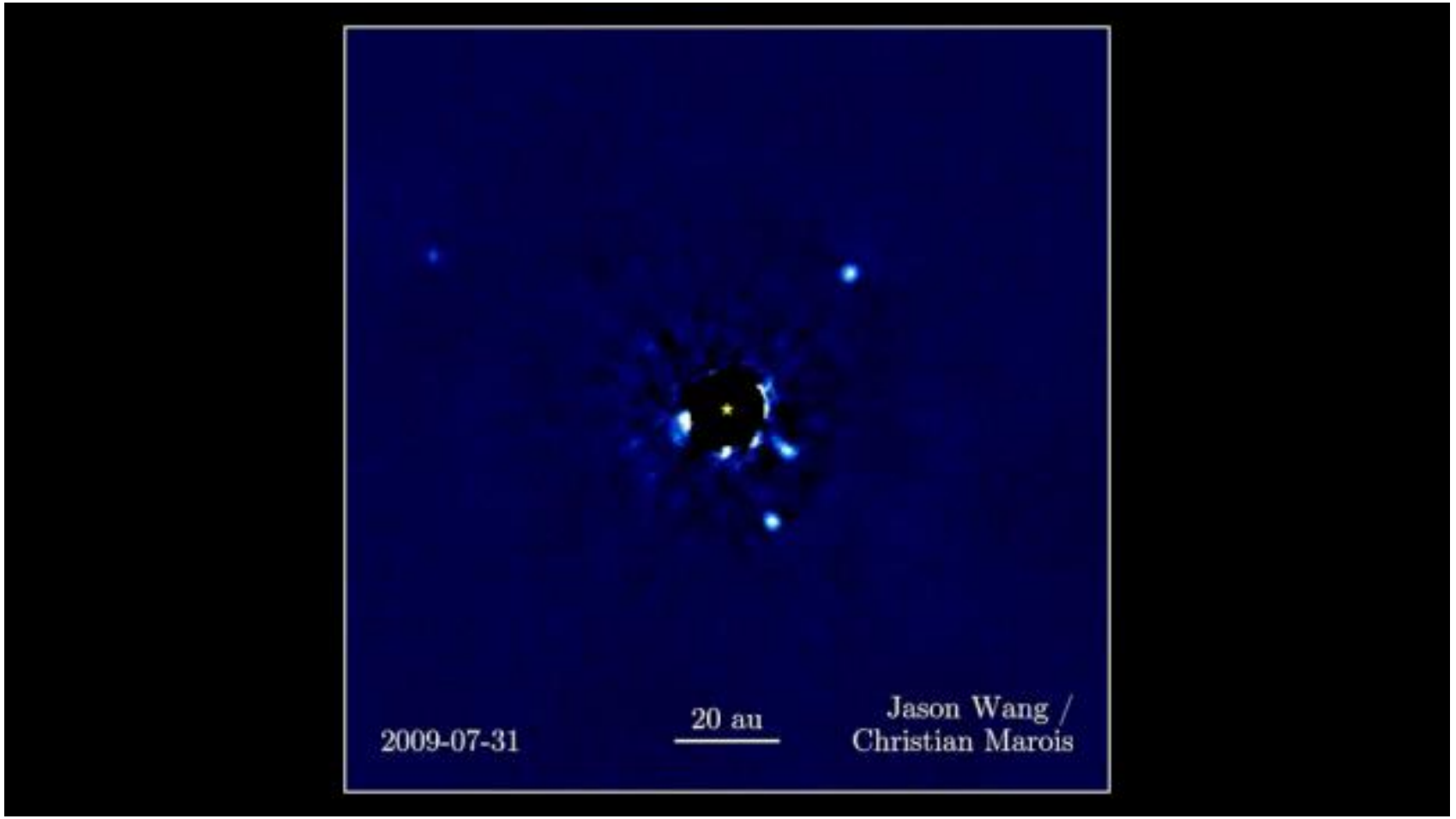
Compact, Low-Power Electronic Readout Systems

Colm Bracken, Eoin Baldwin, Gerhard Ulbricht, Mario de Lucia, Ivan Colantoni, Tom Ray

Presentation Contents

- Brief overview of what we are trying to do with our new instrument
- Requirements for the readout electronics for the DIAS MKIDs Camera
- FPGA board we originally planned to use for our next-gen. readout
- Some of the alternative systems we considered
- COTS (Commercial, Off-The-Shelf) Boards
- Open-Source Firmware Toolflows
- Some affordable boards which may be of interest to the community

Some Direct Imaging to Date



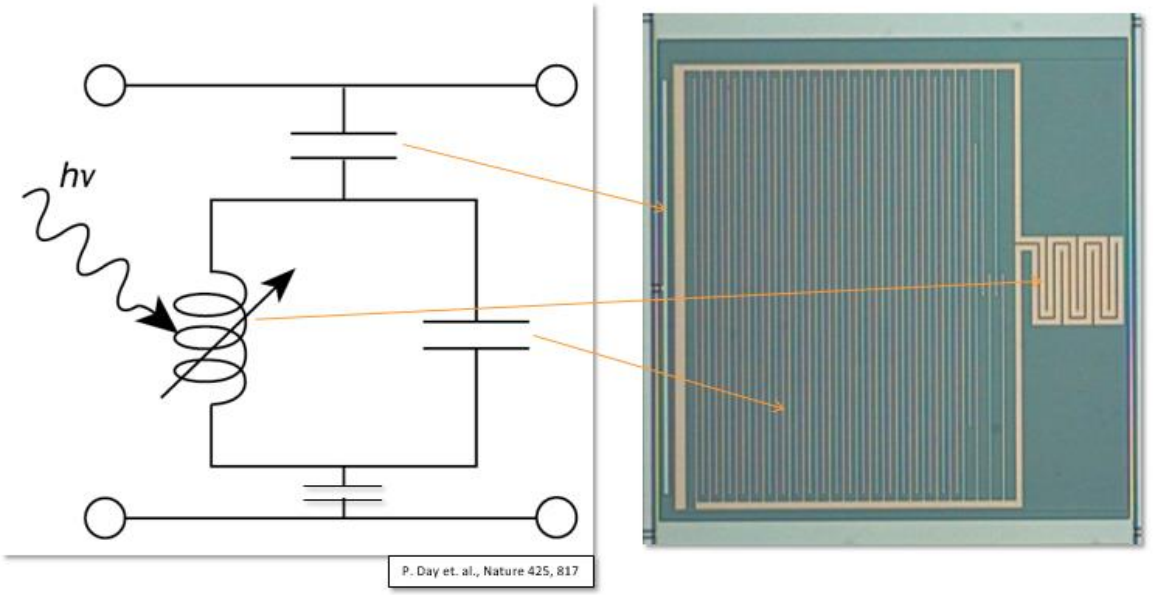
Video credit: **Credit:**J. Wang et al., 2018
https://www.eso.org/public/videos/eso1905b/

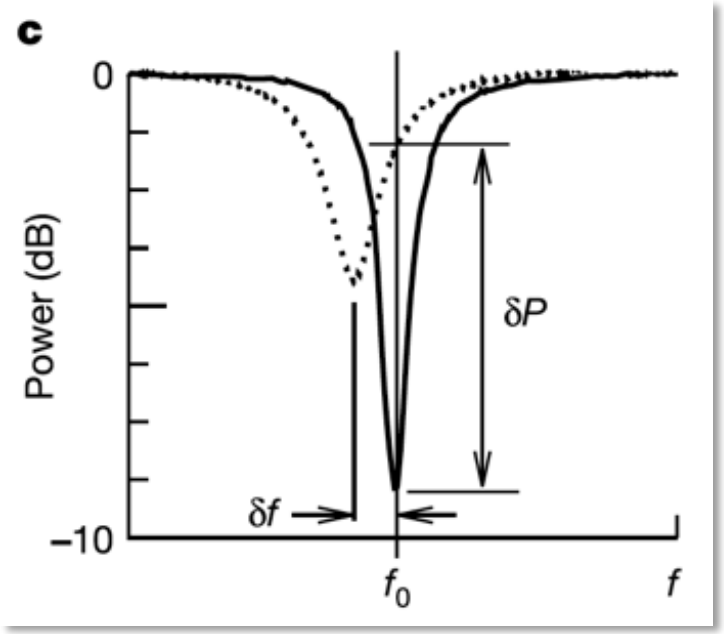
What we want from our new instrument

- Want a focal plane array, with pixel number pushing toward the 100 kilo pixel region (Moderate FoV)
- Want time resolution of ~ 1 microsecond (Photon counting), (Real-time wavefront analysis (for correction with XAO -> Speckle-nulling)
- Each pixel to give spatial and spectral information (IFU without sacrificing 1 dimension (row/column))
- Sensitive to full optical and near-IR wavebands, with high-contrast imaging

- Such an instrument would be well-suited for direct-imaging of exoplanets using large-class ground-based observatories
  - (As discussed during talks earlier)

- Frequency division multiplexing allows MKIDs to scale up to kilo-pixel arrays
- Frequency division multiplexing also allows for a much faster readout (frequency mux intervals rather than time mux intervals)
- Due to the tiny superconducting bandgap (~10^{-4} eV), a single incident photon will generate many quasiparticles -> photon counting & energy-sensitive
- A silicon-based CCD, for example, has a semiconductor bandgap of 1.14 eV



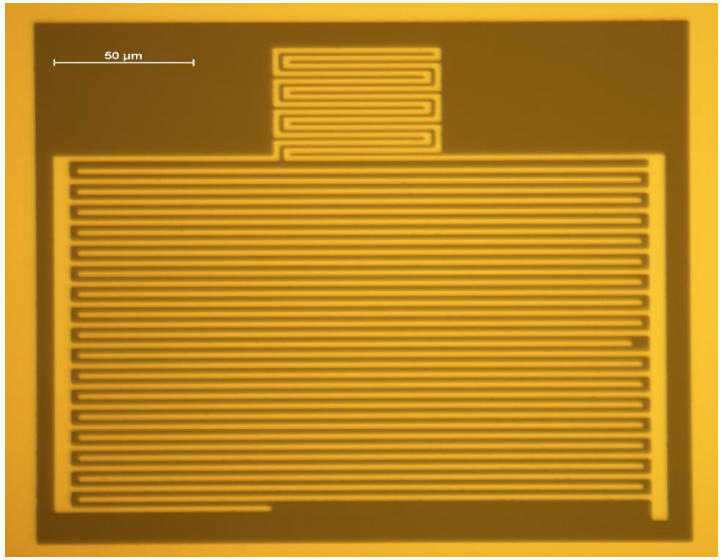


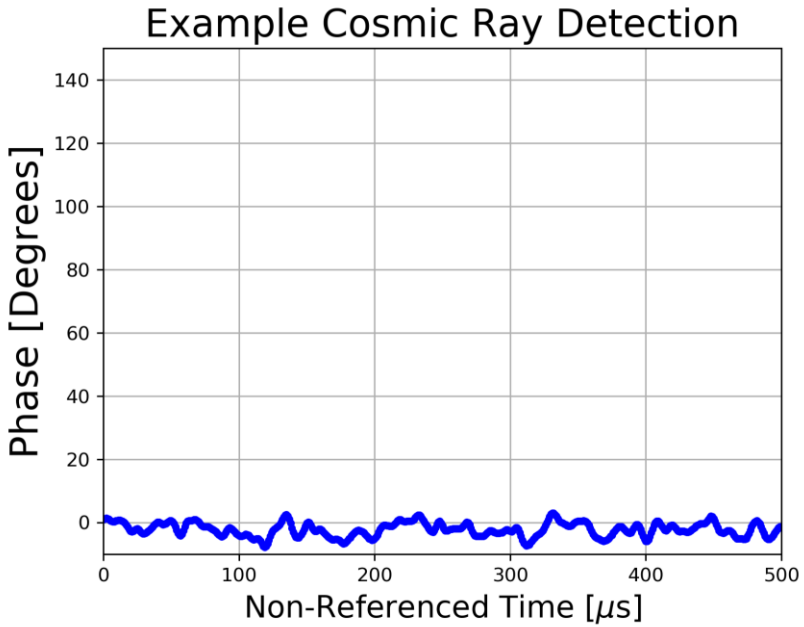
E_{red} ~ 1.5 **eV**

E_{green} ~ 2.5 **eV**

E_{blue} ~ 4.0 **eV**

- Reading out MKIDs using Frequency division multiplexing:
  - Simply monitor the phase of a complex I/Q probe signal, sampling every microsecond





- Reading out MKIDs using Frequency division multiplexing :
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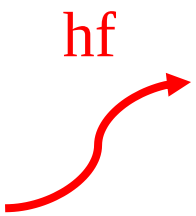
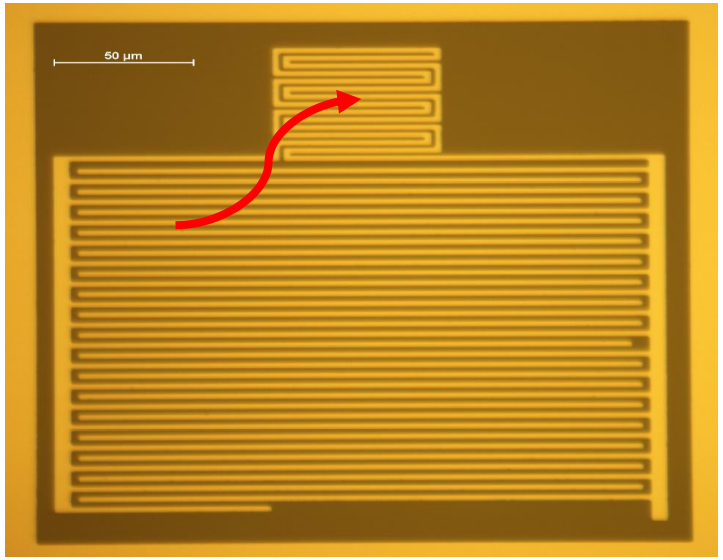
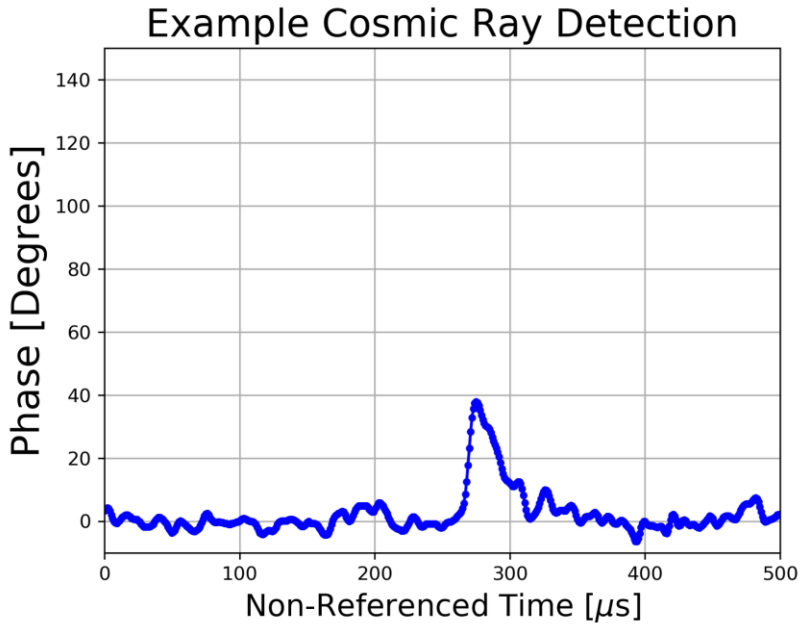
E ~ 1.5 **eV**

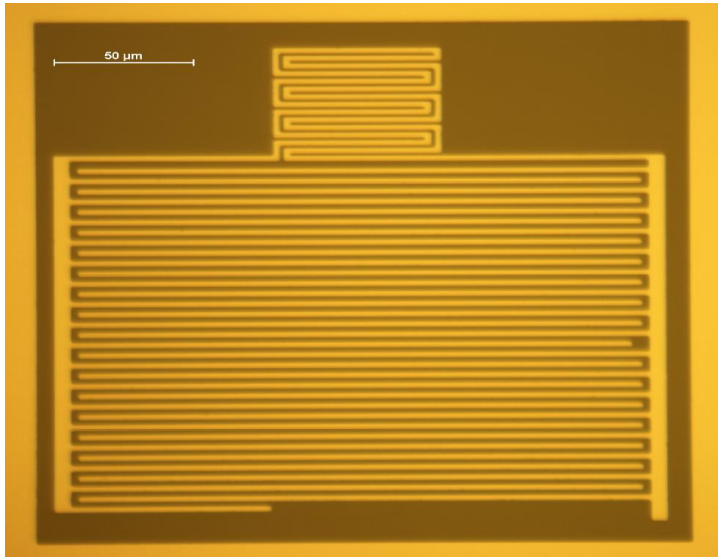
hf

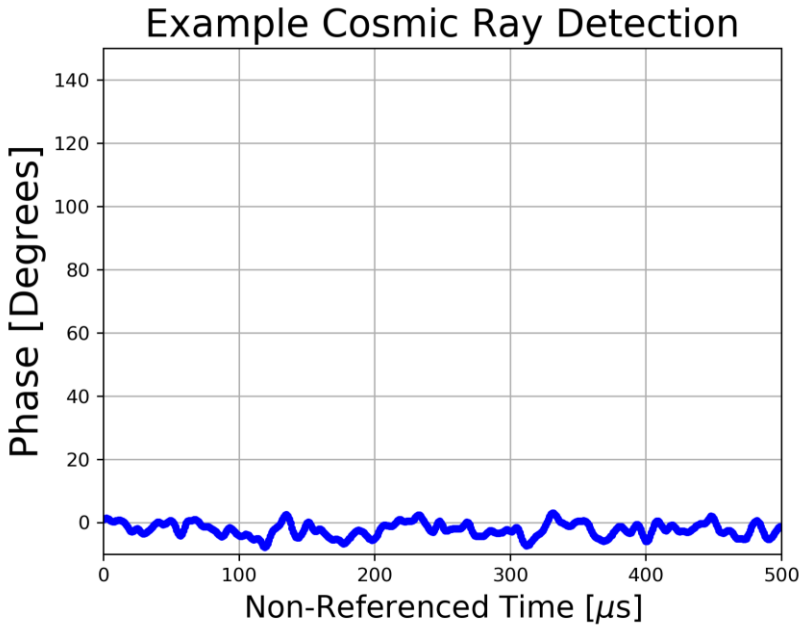






- Reading out MKIDs using Frequency division multiplexing :
  - The higher the energy of the photon, the more Cooper-pairs are broken in the inductor

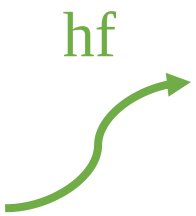


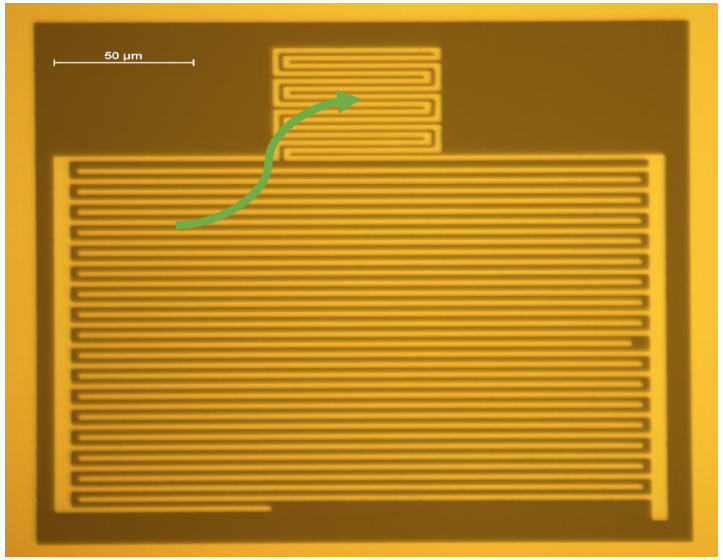


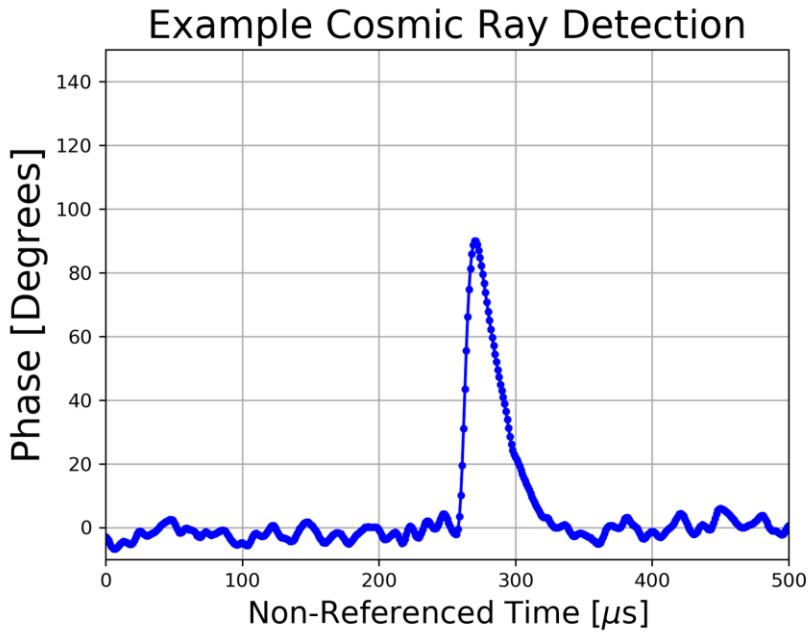
- Reading out MKIDs using Frequency division multiplexing :
  - The higher the energy of the photon, the more Cooper-pairs are broken in the inductor

E ~ 2.5 **eV**

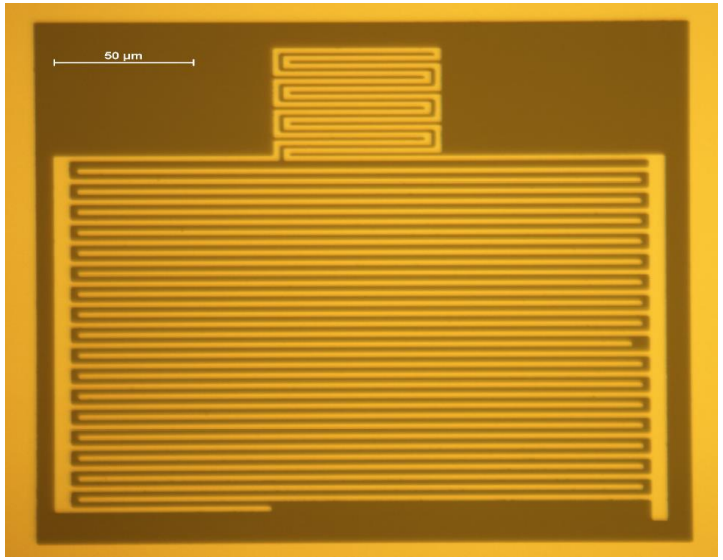
hf

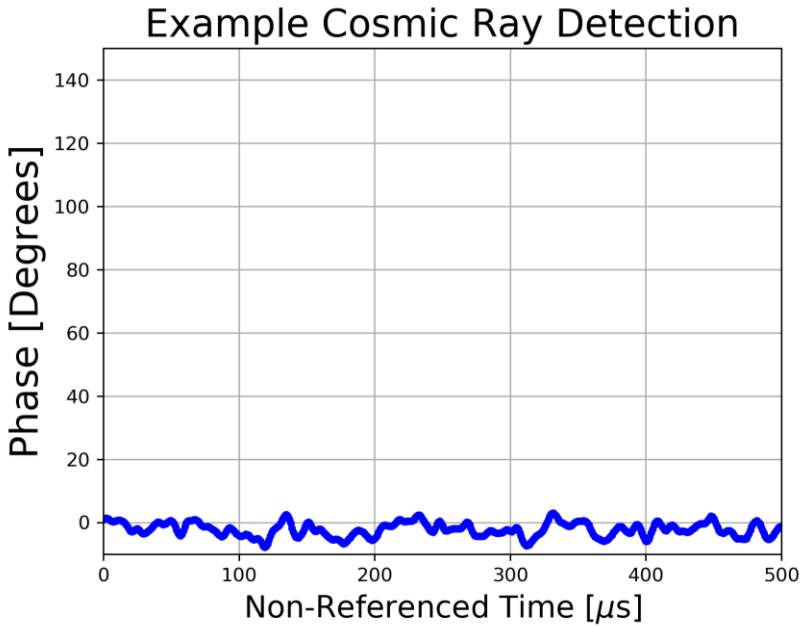




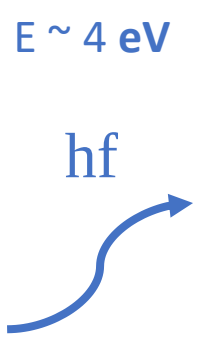


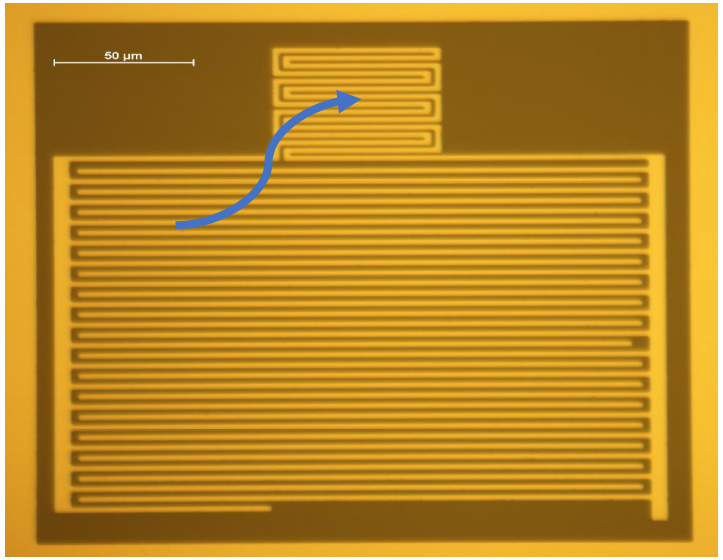
- Reading out MKIDs using Frequency division multiplexing :
  - The more Cooper-pairs that are broken, the larger shift from resonance

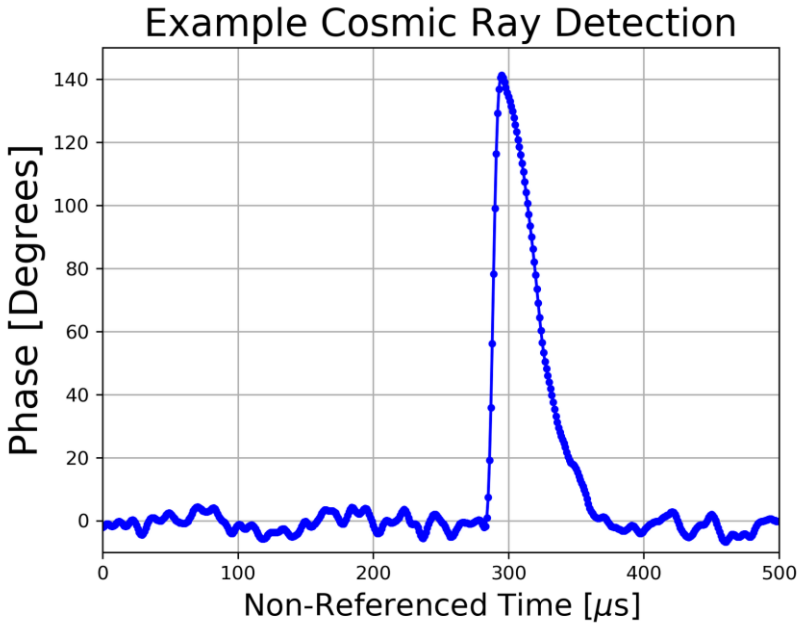




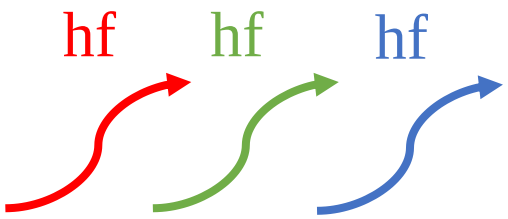
- Reading out MKIDs using Frequency division multiplexing :
  - The larger shift from resonance of the detector, the larger the phase shift of the probe tone

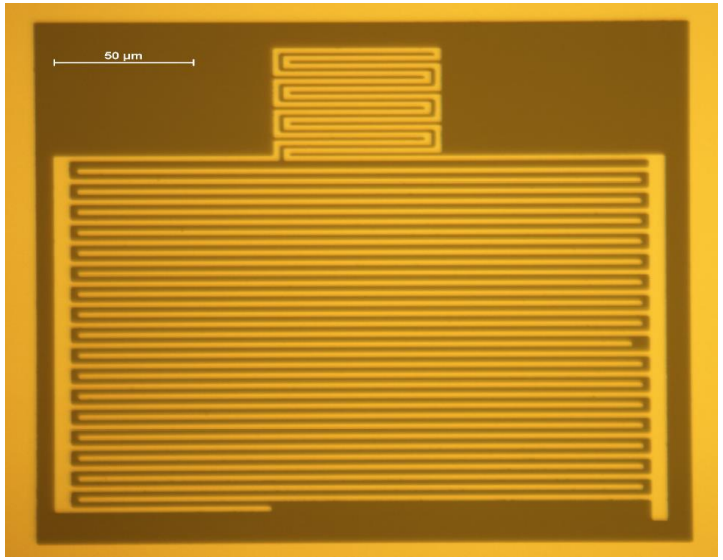


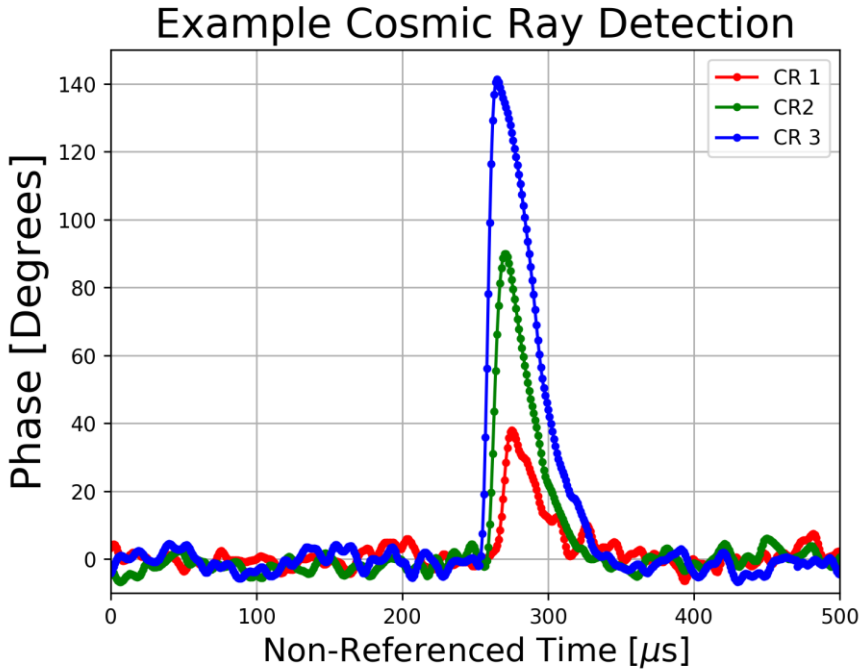




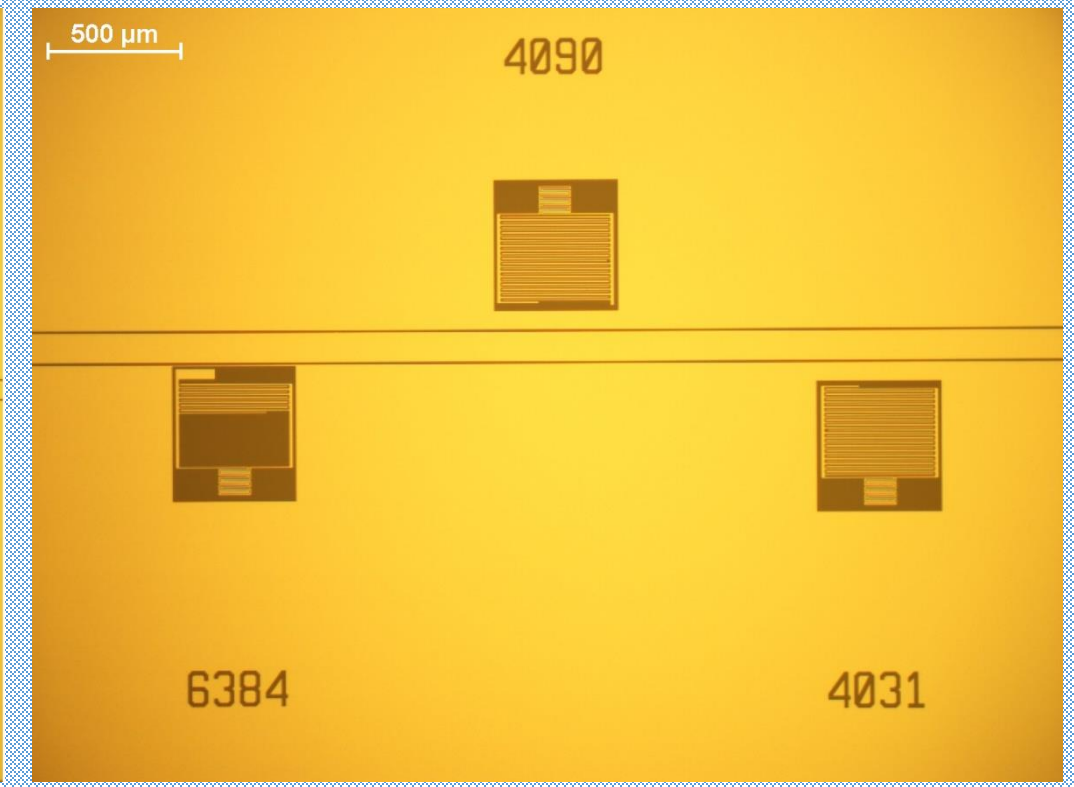
- Reading out MKIDs using Frequency division multiplexing :
  - The larger shift from resonance of the detector, the larger the phase shift of the probe tone



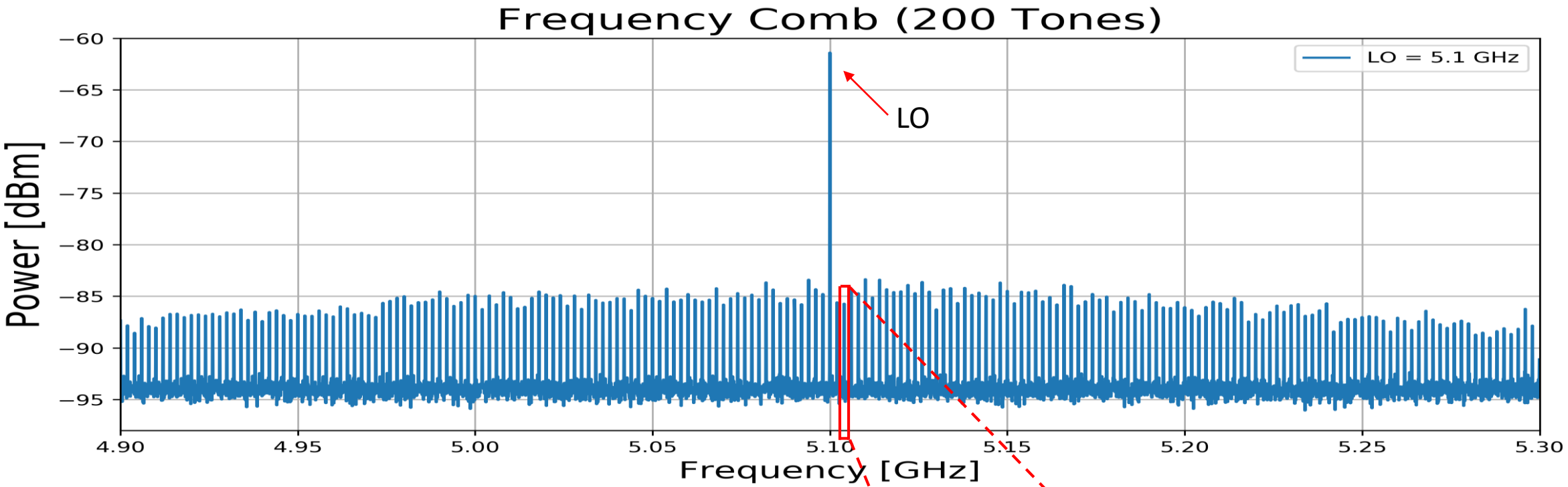


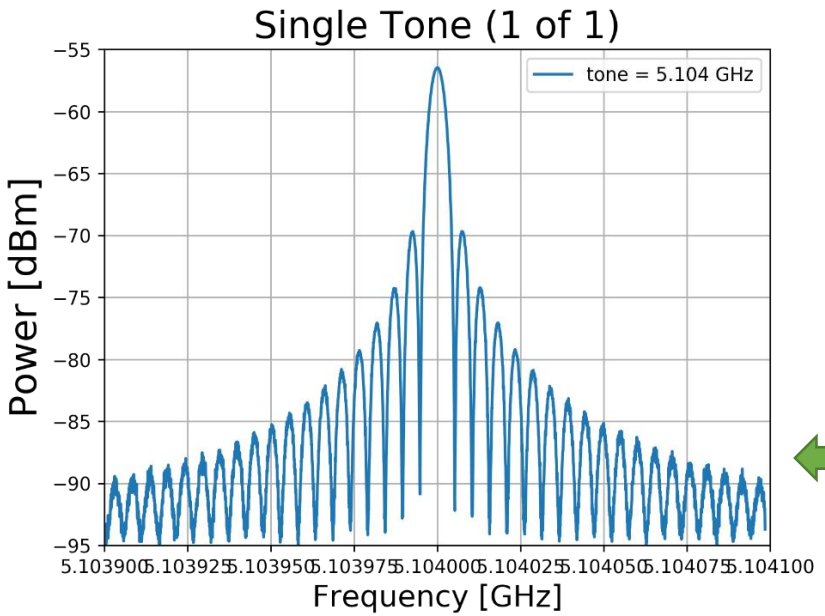


- Fabricating each resonator/pixel with a unique capacitance allows FDM



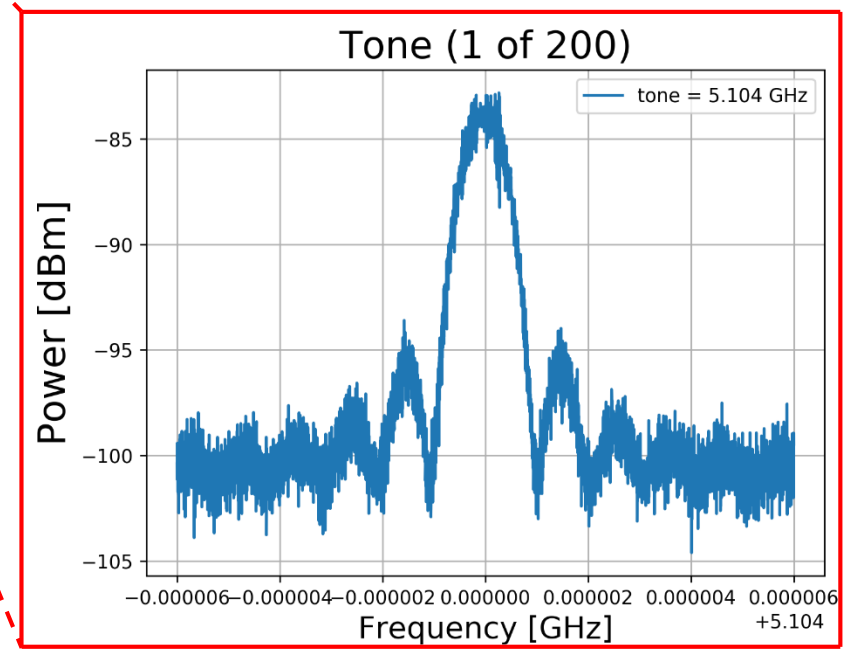
- Driving a large number of resonators is a fairly trivial task – program a DAC to output a ‘frequency comb’ (and up-mix with an LO if necessary)



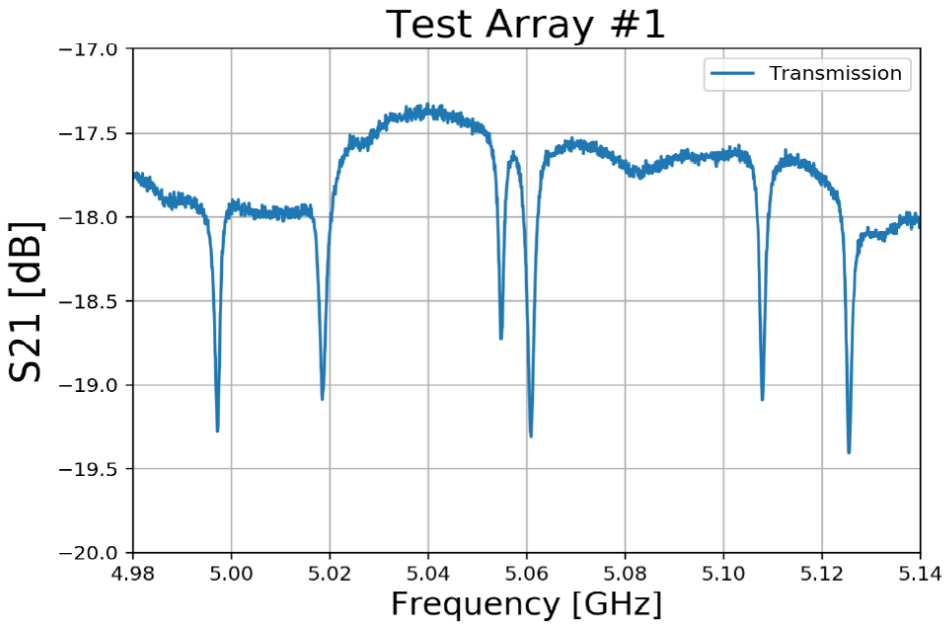


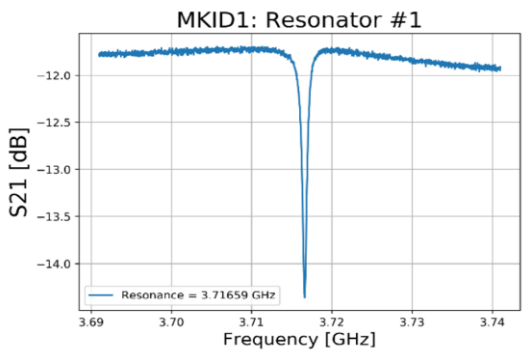
Each ROACH and DAC can output 256 tones with ~ -86 dBm per tone

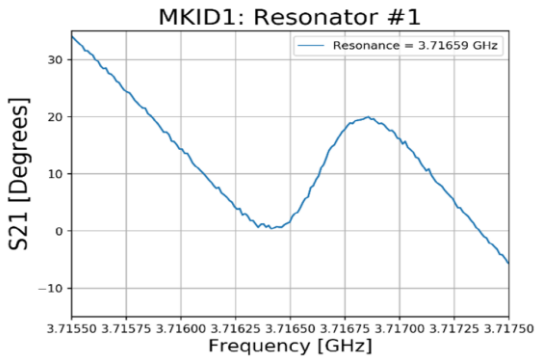
~ -58 dBm for single tone

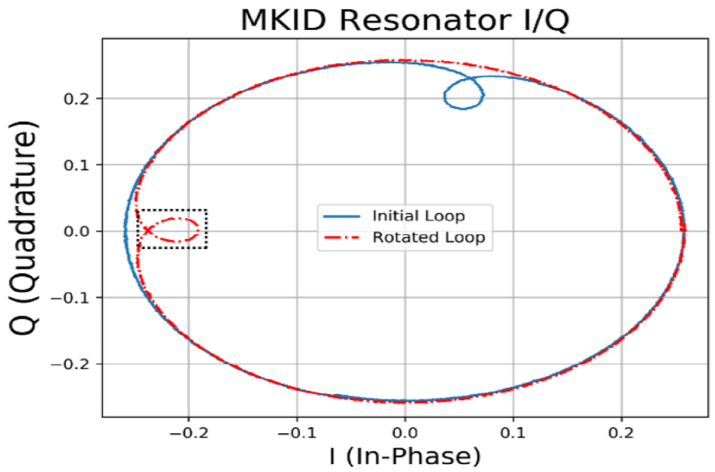


- But separating out each of the many probe tones (channelisation) is not a trivial matter at all…





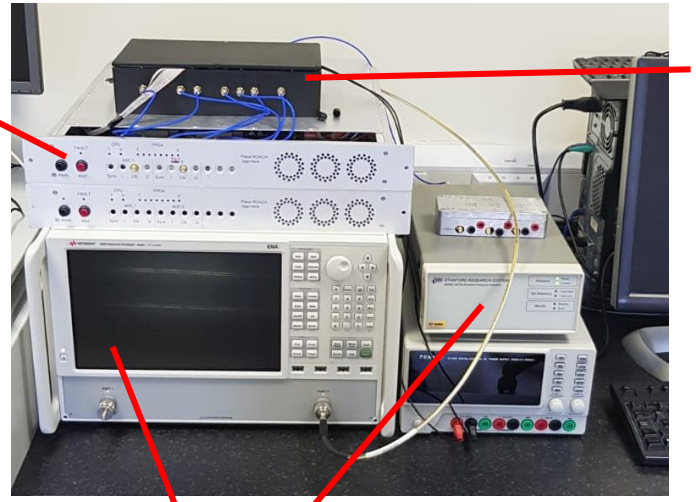




- Computationally demanding task to channelise the tones, and monitor each tone/channel independently for indication of any photon events
- Highly parallel, so either GPUs or FPGAs are best suited

Our Current Readout: ROACH 1 ROACH (Reconfigurable Open-Architecture Computing Hardware) from CASPER

- ROACH 1 FPGA board
- ADC: 550 MSPS, 12 bit
- DAC: 1000 MSPS, 16 bit



- IF/RF Board (&Clock Distribution)

- With these ADCs (550 MSPS) we would need **8 full systems** to take full advantage of the 2,000 probe tones per feedline

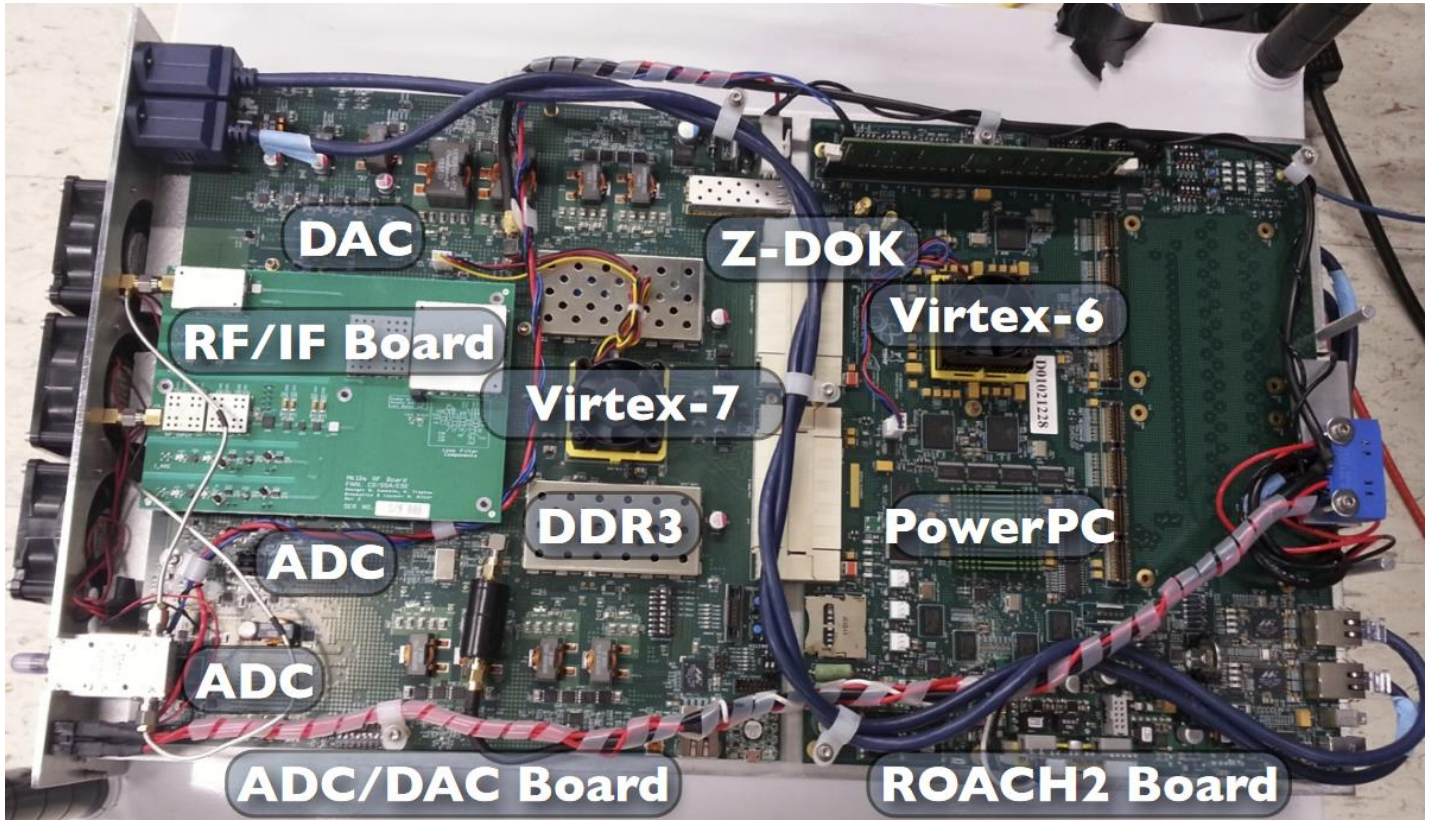
- Each ROACH 1 can read ~ 250 pixels
- Cost per pixel ~ € 22.00 pp

- Rubidium Frequency Standard (Stable 10 MHz) & 1PPS
- VNA

CASPER (Collaboration for Astronomy Signal Processing and Electronics research)

State of the Art MKID Readout (for UV/O/IR)

- UCSB/Mazin Labs, & FermiLab
- CASPER Board
- ROACH 2 FPGA board
- ADC: 2 GSPS, 12 bit
- DAC: 2 GSPS, 16 bit



A single ROACH 2 based MKID readout, M. Strader, 2016

- Each ROACH 2 can read ~ <u>1,000 pixels</u>

State of the Art MKID Readout (for UV/O/IR)

- UCSB/Mazin Labs, & FermiLab
- DARKNESS MKID Instrument: 10 x ROACH 2 (10,000 pixels)
- DARKNESS is commissioned, and doing Science at Palomar Observatory
- UCSB Group already commissioning their next MKID camera: MEC (MKID Exoplanet Camera)
- MEC has 20 x ROACH 2 boards, for 20,000 pixels

DARKNESS Readout Stack, M. Strader, 2016

Original Plan for Gen 3 Readout

- Originally had planned to use the ROACH 3 (or SKARAB) board, developed for SKA
- The channelisation routines we employ are similar to SKA digital spectrometers
- So made some sense to continue using SKA/CASPER boards and software
- However, having looked into the SKARAB boards, they were very expensive, and not ideal for our use for a GEN 3 MKID readout

SKARAB Board, for SKA-SA Digital Spectrometer.
Image Credit: Peralex, South Africa.

SKARAB/ROACH 3 (Peralex – SKA-SA)

Component	No. Pixels	Unit Price [Euro]	Total Price (with ADCs etc.) [Euro]	Sub-Total [Euro]
SKARAB	FPGA Baseboard	10,693	1	10,693
Peralex 3 GSPS ADC	A/D Converter	4,830	2	9,660
FMC230 5.7 GSPS DAC	D/A Converter	2,600	1	2,600
VP780 FPGA Carrier	FPGA Baseboard	11,250	1	11,250
IF Board	LO and Mixer	~ 5,000	1	~ 5,000
Total				~ 39,203

Number of Channels: 1,500

Cost per Pixel: € 26.14

http://www.tauceti.caltech.edu/casper-workshop-2017/slides/2_new.pdf

MKID Readout Wish-List (*and Bottlenecks*)

- Currently, need **tones ~ 2 MHz apart** (based on resonator Q-factors)
- Simple math: **500 resonators/tones per GHz** of RF bandwidth (per coax)
- Constrained to **1 octave of RF bandwidth**: Current best option is **4 – 8 GHz** (available low-T amps)
- So, for each feedline, we want **2,000 probe tones/comb over 4 – 8 GHz**
- Sensible to work at lower base frequencies: use I/Q-mixing: **(-2 to +2 GHz, BB**)
- Of course, Nyquist criteria: For 2 GHz RF, we need **4 GSPS sampling rates for our ADCs** (maybe more for our DACs)
- Ultimately, we want to independently monitor phase of each tone over time, with time resolution of ~ 1 microsecond (Thus, **huge FPGA resources** required!!!)
- **Minimal Mass/Footprint, Power, and of course Cost-per-Pixel!!!**

Summary of Trade-Off Analysis

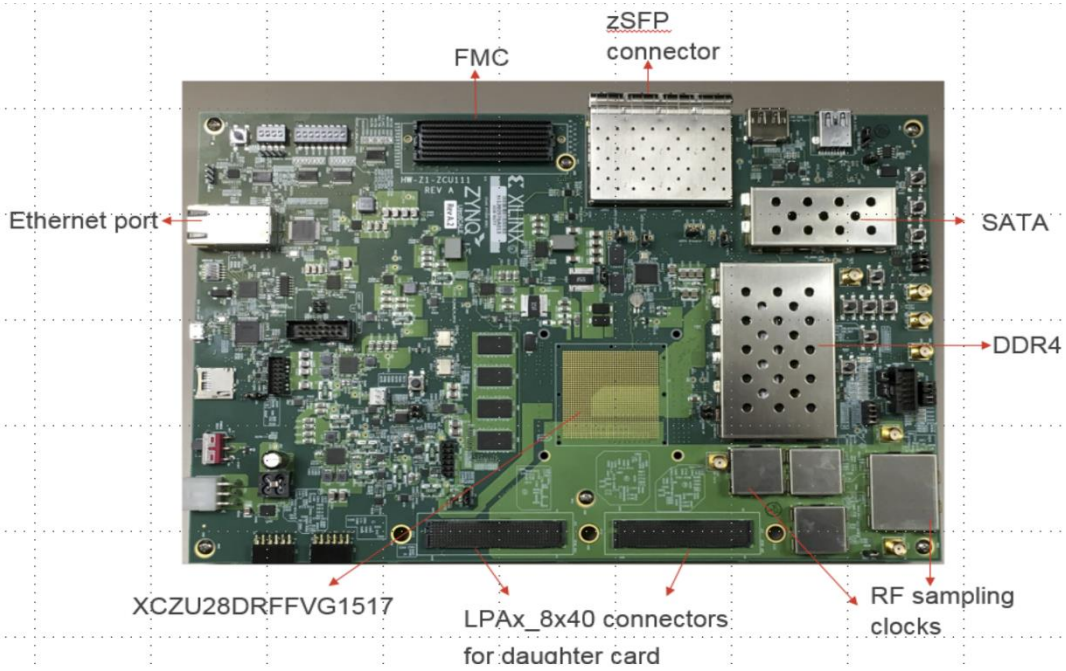
FPGA Carrier Board	Description	Unit Price [Euro]	Total Price (with ADCs etc.) [Euro]	No. of Pixels/Channels per Board	Total Cost-per-Pixel [Euro]
SKARAB (SKA)	FPGA Baseboard	10,693	39,203	1,500	**26.14**
UniBoard II (SKA)	FPGA Baseboard	~ 20,000	~ 39,500	➢ 2,000	**19.75**
AASL Custom Board (SKA)	FPGA Baseboard	~ 15,000	➢ 34,500	➢ 2,000	➢ **17.25**
Abaco VP880 (SRON System)	FPGA Baseboard	14,800	~ 45,550	➢ 2,000	**22.78**
Xilinx VCU118 Eval Kit COTS	FPGA Baseboard	5,800	25,300	➢ 2,000	**12.65**
Xilinx ZCU111 COTS	FPGA Baseboard + RF SoC	8,995	18,000 – 28,000	4,000 – 8,000	**3.62 – 4.75**
Abaco VP430 COTS	FPGA Baseboard + RF SoC	25,000	67,000	4,000 – 8,000	**8.38 – 16.75**
Vadatech AMC599 (EW)	FPGA Baseboard + RF SoC	~ 20,000	~ 27,800	➢ 3,000	**9.27**

Xilinx ZCU111 COTS Board (RF SoC)

Component	Description	Unit Price [Euro]	Quantity	Sub-Total [Euro]
Xilinx RF-SoC Dev Board	FPGA ADCs/DACs	8,995	1	8,995
IF Boards	LO and Mixer	~ 5,000	2/4	~ 10,000/ 20,000
Total				18,995/ 28,995

Number of Channels: > 8,000 (Potentially)

Cost per Pixel: € 3.62 – € 4.75 (XUP Donation Program?)



Xilinx: Zynq RF SoC: https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html

Xilinx Zynq RF SoC: Potentially 8,000 pixels!

Xilinx: Zynq RF SoC: https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html

- With the on-board 8 x 6.4 GSPS DACs and 8 x 4 GSPS ADCs, we could potentially read 8,000 MKIDs
- However, FPGA resources on chip will not allow this
- Should be ok for F-Engine DSP of 8,000 channels
- But, if the 8,000 DDC's are needed then much more DSP capacity is needed. Also, memory requirements?
- We will likely need the FMC+ port for HMC
- Cost per/pixel: ~ **€ 3.62 – € 4.75**
  - **Could be significantly less if/when Xilinx include these boards on their XUP University Donation Program…**

What Makes This Board So Good?

ZCU111 Evaluation Board

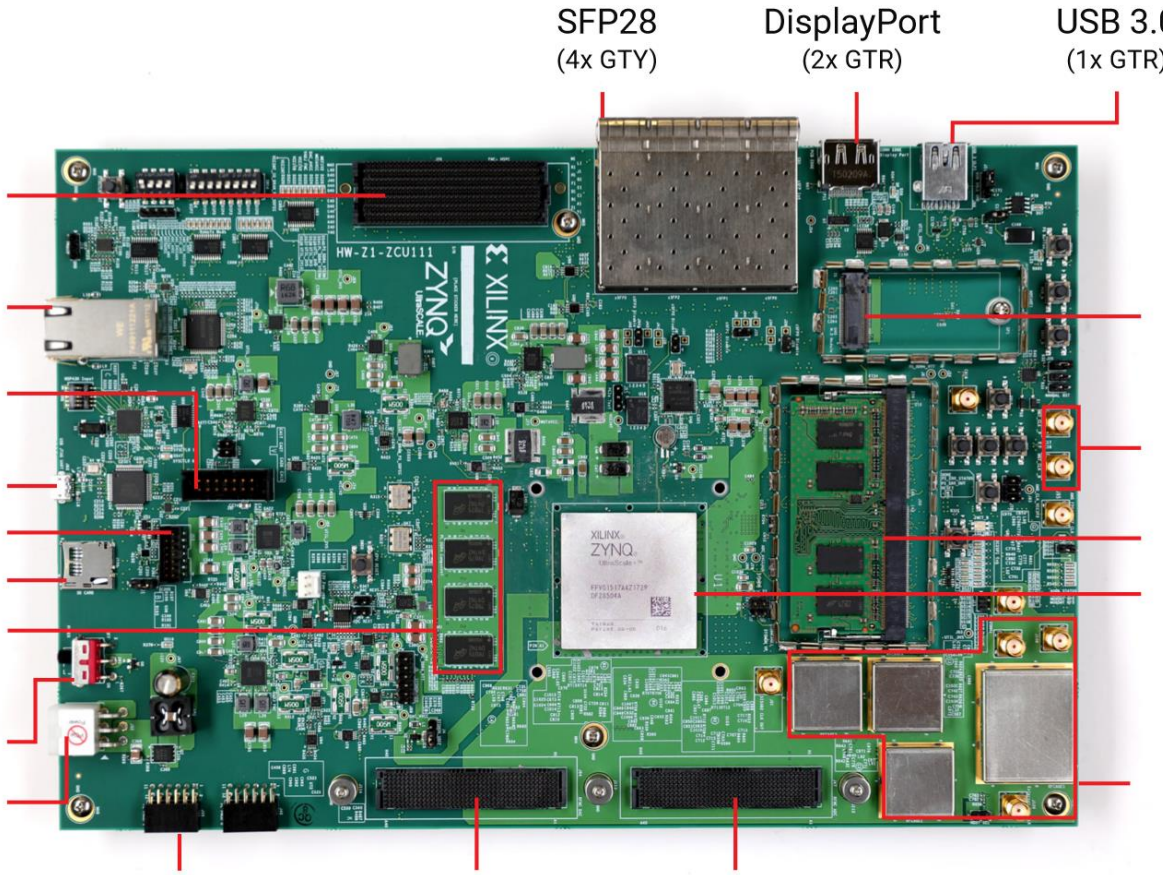
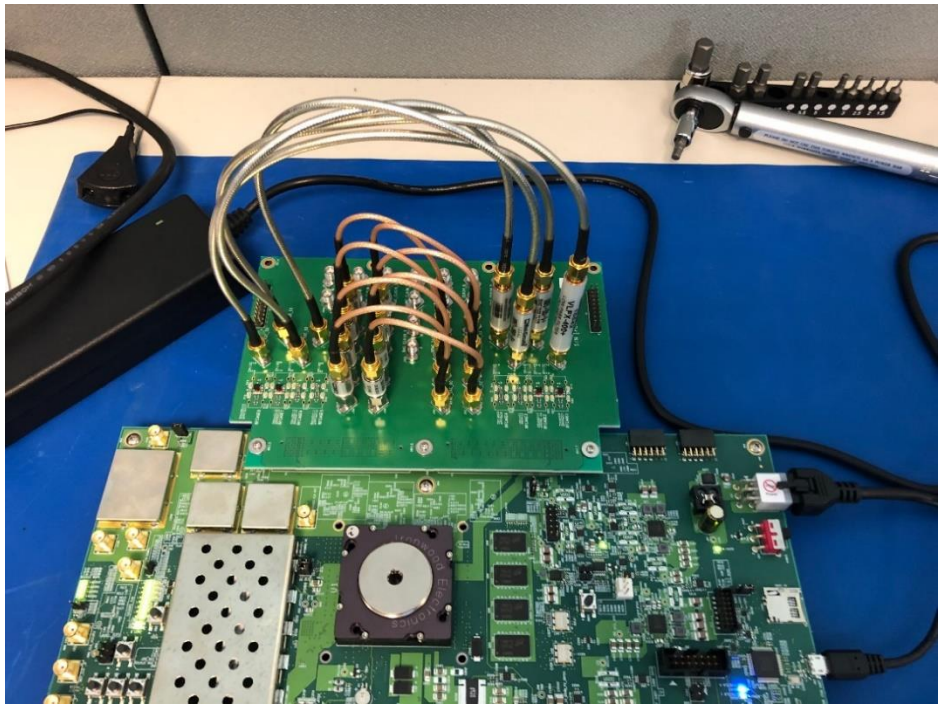


Image Credit: Cathal McCabe Xilinx

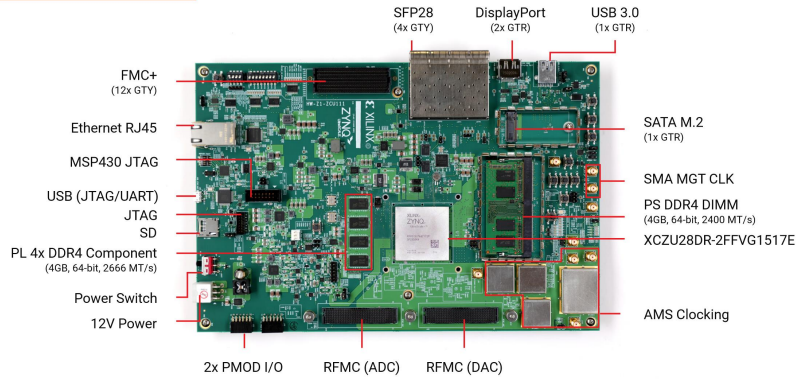
Xilinx Zynq RF SoC: Potentially 8,000 pixels!!!



- The 8 x 6.4 GSPS DACs and 8 x 4 GSPS ADCs, are housed on the actual chip
- Not only does this make the system compact – its significantly reduces power
- The extremely high sample rates of the data converters is achieved through high interleaving
- However, tests have shown that there is very low spurious noise – ADCs look great!

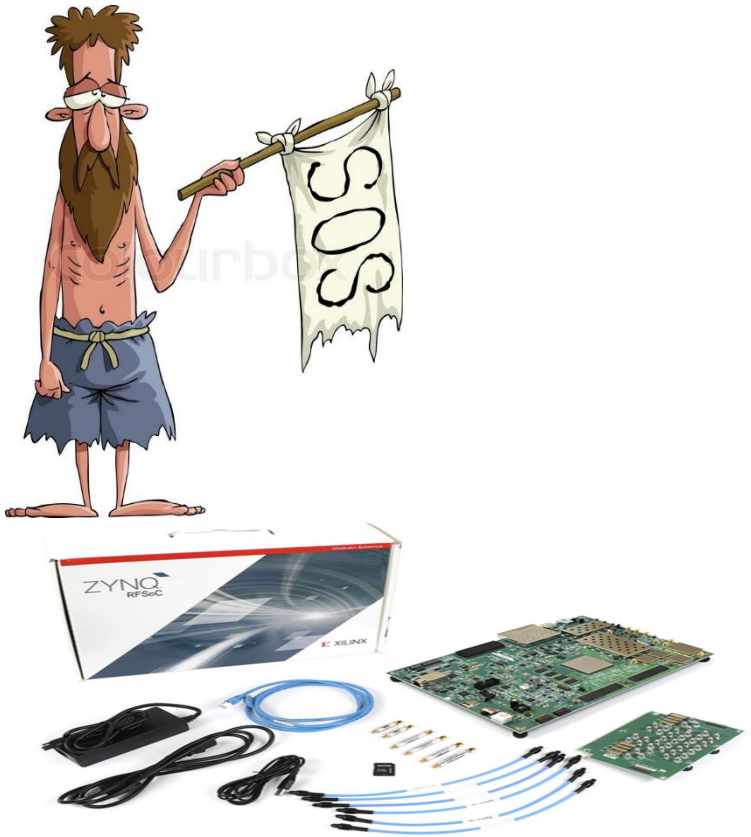
So, we've gone and bought one of these boards… *now what*?

ZCU111 Evaluation Board



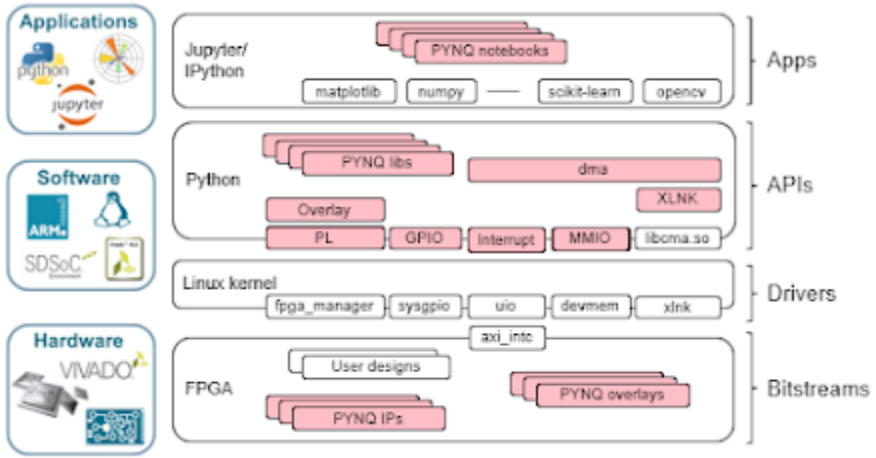
- Like many of these (quite complex) FPGA evaluation boards, it is difficult to know where to start with programming it
- The nice thing about using a ROACH 1 or ROACH 2 – They are CASPER boards (Support!)
- CASPER (Collaboration for Astronomy Signal Processing and Electronics research)
- CASPER started in Berkley (~ 15 years ago)
- Other institutes/nations joined, with South Africa now a big contributor to their activities
- Now in fact, the 'C' in CASPER is really more for Community rather than Collaboration

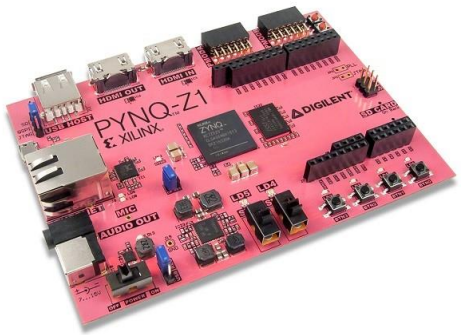
Decided to ask for Help



- We went to the CASPER group, and asked if they would be interested in '*CASPERising*' this exciting new FPGA/RF SoC board
- It turned out that we weren't the only ones hoping to program this board with the CASPER approach
- So, in June of this year, we went to South Africa (with our board), in the hopes of developing a fully functional readout firmware within a 1 week workshop
- Unfortunately we were being a little overly-optimistic
- It turns out the new RF SoC chip is a little tricky to work with (even for the CASPER expert firmware developers)

Other open-source toolflows/approaches





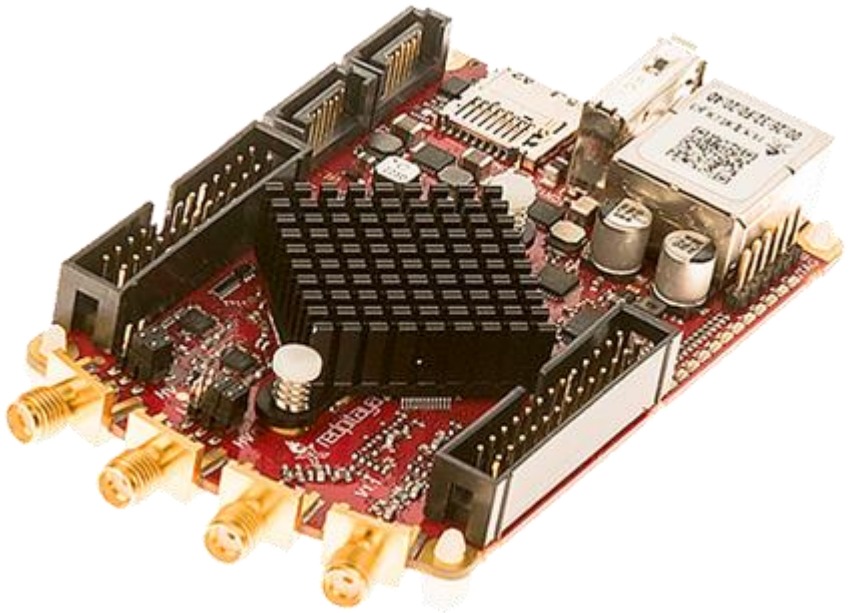
python™

jupyter

Linux

- There are likely alternative open-source programming approaches
- One we are now using (for the short-term), while we try to CASPERise the board (longer-term), is PYNQ
- PYNQ (or, Python for Zynq) is an open-source programming environment for developing bit-stream firmware files for the new Zynq-class Xilinx chips
- It is quite user-friendly, and all control software is done through Python's **Jupyter Lab** (Very similar to **Jupyter Notebook**)
- University of Strathclyde, Glasgow, and Xilinx themselves have developed a few nice firmware templates, including a QPSK model

Other boards worth mentioning



The Red Pitaya. Image Credit: STEMlab https://www.redpitaya.com

- If you have a readout electronics project, which is a little more demanding than what's possible with a Raspberry Pi, or Arduino, the Red Pitaya is worth exploring
- For example: SDR Transceiver, Data Acquisition, Digital Spectrometer, Oscilloscope, VNA, etc.
- It has a Zynq chip on-board, so it should be supported by PYNQ
- On-chip data converters (few hundred MSPS)
- The CASPER group has taken a keen interest in the Red Pitaya (mostly for student projects and tutorials), and it is now fully CASPERised

Many Thanks!
Questions Welcome.

- Queries to: cbracken@cp.dias.ie